

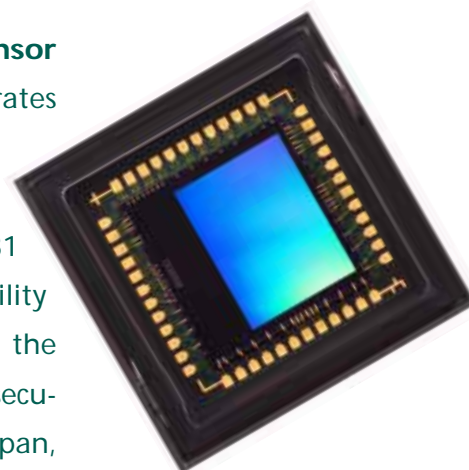


## MT9P031: 1/2.5-Inch 5-Mp Digital Image Sensor

# MT9P031 Image Sensor

## Product Brief

Micron's MT9P031 is a 1/2.5-inch CMOS digital image sensor with an active-pixel array of 2592H x 1944V. It incorporates sophisticated camera functions such as windowing, binning, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface. The MT9P031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and commercial security applications, including high resolution network cameras; pan, tilt, and zoom cameras; and hybrid video/still cameras.



## Applications

- High-resolution network cameras
- Wide field of view cameras
- High-definition surveillance camera
- Dome cameras with electronic pan, tilt, and zoom
- Hybrid video cameras with high resolution stills
- Detailed feature extraction for smart cameras

## Features

- Micron<sup>®</sup> DigitalClarity<sup>®</sup> imaging technology
- High frame rate
- Superior low-light performance
- Low dark current
- Global reset release, which starts the exposure of all rows simultaneously
- Bulb exposure mode, for arbitrary exposure times
- Snapshot mode to take frames on demand
- Horizontal and vertical mirror image
- Column and row skip modes to reduce image size without reducing field of view
- Column and row binning modes to improve image quality when resizing
- Simple two-wire serial interface
- Subframe windowed readout
- Programmable controls: gain, frame rate, frame size, exposure
- Automatic black level calibration
- On-chip PLL

### Key Parameters

Optical format	1/2.5-inch (4:3)	
Active imager size	5.70mm(H) x 4.28mm(V) 7.13mm diagonal	
Active pixels	2592H x 1944V	
Pixel size	2.2 $\mu$ m x 2.2 $\mu$ m	
Color filter array	RGB Bayer pattern	
Shutter type	Global reset release (GRR), snapshot only; electronic rolling shutter (ERS)	
Maximum data rate/ master clock	96 Mp/s at 96 MHz (2.8V I/O) 48 Mp/s at 48MHz (1.8V I/O)	
<b>Frame Rate</b>		
Full resolution	Programmable up to 14 fps	
VGA (with binning)	Programmable up to 53 fps	
720P (1280 X 720, skipping mode)	Programmable up to 60 fps	
ADC resolution	12-bit, on-chip	
Responsivity	1.4 V/lux-sec (550nm)	
Pixel dynamic range	70.1dB (full resolution), 76dB (2 x 2 binning)	
SNR <sub>MAX</sub>	38.1dB (full resolution), 44dB (2 x 2 binning)	
Supply voltage	I/O	1.7V–3.1V
	Digital	1.7V–1.9V (1.8V nominal)
	Analog	2.6V–3.1V (2.8V nominal)
Power consumption	381mW at 14 fps full resolution	
Operating temp.	–30°C to +70°C	
Packaging	48-pin iLCC, die	
Output gain	10 e-/LSB	
Read noise	2.6 e-RMS at 16X	
Dark current	25 e-/pix/s at 55C	



### Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array, and is typically equal to 1 EXTCLK period. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (<sup>t</sup>ROW) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 8.

**Table 8: Frame Time**

Parameter	Name	Equation	Default Timing at EXTCLK = 96 MHz
fps	Frame Rate	$1/{}^t\text{FRAME}$	14
<sup>t</sup> FRAME	Frame Time	$(H + \max(\text{VB}, \text{VBMIN})) \times {}^t\text{ROW}$	71.66ms
<sup>t</sup> ROW	Row Time	$2 \times {}^t\text{PIXCLK} \times \max(\left(\frac{W}{2} + \max(\text{HB}, \text{HBMIN})\right), (41 + 346 \times (\text{Row\_Bin} + 1) + 99))$	36.38µs
W	Output Image Width	$2 \times \text{ceil}\left(\frac{\text{Column\_Size} + 1}{2 \times (\text{Column\_Skip} + 1)}\right)$	2592 PIXCLK
H	Output Image Height	$2 \times \text{ceil}\left(\frac{\text{Row\_Size} + 1}{2 \times (\text{Row\_Skip} + 1)}\right)$	1944 rows
SW	Shutter Width	$\max(1, (2 * 16 \times \text{Shutter\_Width\_Upper} + \text{Shutter\_Width\_Lower}))$	1943 rows
HB	Horizontal Blanking	$\text{Horizontal\_Blank} + 1$	1 PIXCLK
VB	Vertical Blanking	$\text{Vertical\_Blank} + 1$	26 rows
HBMIN	Minimum Horizontal Blanking	$346 \times (\text{Row\_Bin} + 1) + 64 + (W_{\text{dc}} / 2)$	450 PIXCLK
VBMIN	Minimum Vertical Blanking	$\max(8, \text{SW} - H) + 1$	9 rows
<sup>t</sup> PIXCLK	Pixclk Period	$1/{}^t\text{PIXCLK}$	10.42ns

The minimum horizontal blanking (HBMIN) values for various Row\_Bin and Column\_Bin settings are shown in Table 9.

**Table 9: HB<sub>MIN</sub> Values for Row\_bin vs. Column\_bin Settings**

		Column_bin (Wdc)		
		0	1	3
Row_b in	0	450	430	420
	1	796	776	766
	3	1488	1468	1458



**Frame Rates at Common Resolutions**

Table 10 and Table 11 show examples of register settings to achieve common resolutions and their frame rates. Frame rates are shown both with subsampling enabled and disabled.

**Table 10: Standard Resolutions**

Resolution	Frame Rate	Sub-sampling Mode	Column Size (R0x04)	Row Size (R0x03)	Shutter Width_Lower (R0x09)	Row_Bin (R0x22 [5:4])	Row_Skip (R0x22 [2:0])	Column_Bin (R0x23 [5:4])	Column_Skip (R0x23 [2:0])
2592 x 1944 (Full Resolution)	14	N/A	2591	1943	<1943	0	0	0	0
2048 x 1536 QXGA	21	N/A	2047	1535	<1535	0	0	0	0
1600 x 1200 UXGA	31	N/A	1599	1199	<1199	0	0	0	0
1280 x 1024 SXGA	42	N/A	1279	1023	<1023	0	0	0	0
1024 x 768 XGA	63	N/A	1023	767	<767	0	0	0	0
	63	skipping	2047	1535		0	1	0	1
	47	binning	2047	1535		1	1	1	1
800 x 600 SVGA	90	N/A	799	599	<599	0	0	0	0
	90	skipping	1599	1199		0	1	0	1
	65	binning	1599	1199		1	1	1	1
640 x 480 VGA	123	N/A	639	479	<479	0	0	0	0
	123	skipping	2559	1919		0	3	0	3
	53	binning	2559	1919		3	3	3	3

**Table 11: Wide Screen (16:9) Resolutions**

Resolution	Frame Rate	Sub-sampling Mode	Column Size (R0x04)	Row Size (R0x03)	Shutter Width_Lower (R0x09)	Row_Bin (R0x22 [5:4])	Row_Skip (R0x22 [2:0])	Column_Bin (R0x23 [5:4])	Column_Skip (R0x23 [2:0])
1920 x 1080 HDTV	31	N/A	1919	1079	<1079	0	0	0	0
1280 x 720 HDTV	60	N/A	1279	719	<719	0	0	0	0
	60	skipping	2559	1439	<719	0	1	0	1
	45	binning	2559	1439	<719	1	1	1	1

Notes: 1. It is assumed that the minimum horizontal blanking and the minimum vertical blanking conditions are met, and that all other registers are set to default values.

## Ordering Information

Table 1: Available Part Numbers

Part Number	Description
MT9P031I12STC ES	48-Pin iLCC 7 deg
MT9P031I12STD ES	Demo kit
MT9P031I12STH ES	Demo kit headboard

## General Description

The MT9P031 sensor can be operated in its default mode or programmed for frame size, exposure, gain setting, and other parameters. The default mode outputs a full-resolution image at 14 frames per second (fps).

An on-chip analog-to-digital converter (ADC) provides 12 bits per pixel. FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, as is a pixel clock that is synchronous with valid data.

The 5-megapixel CMOS image sensor features DigitalClarity—Micron’s breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Figure 1: MT9P031 Quantum Efficiency versus Wavelength

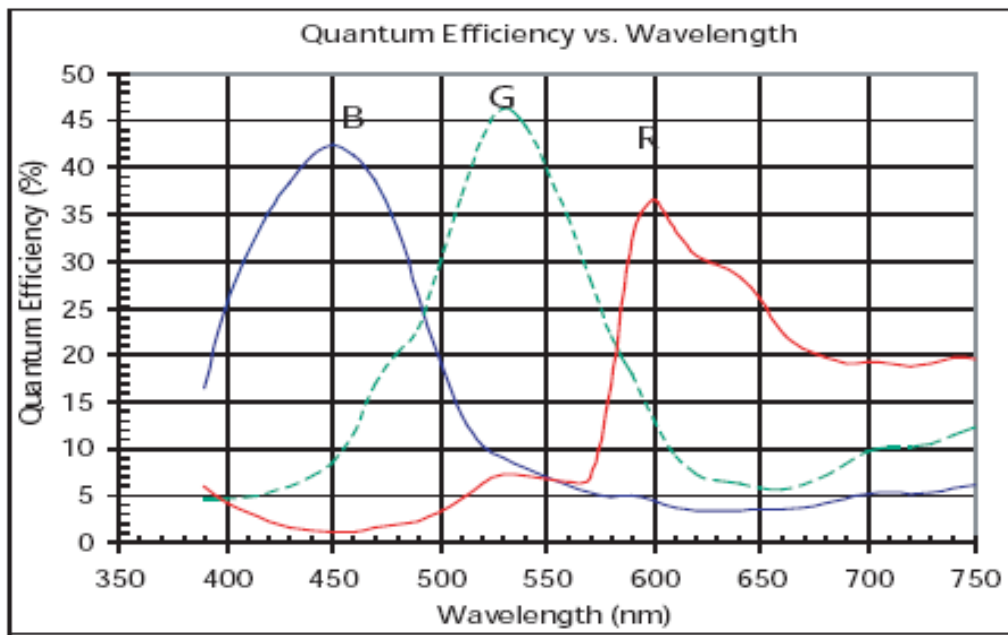
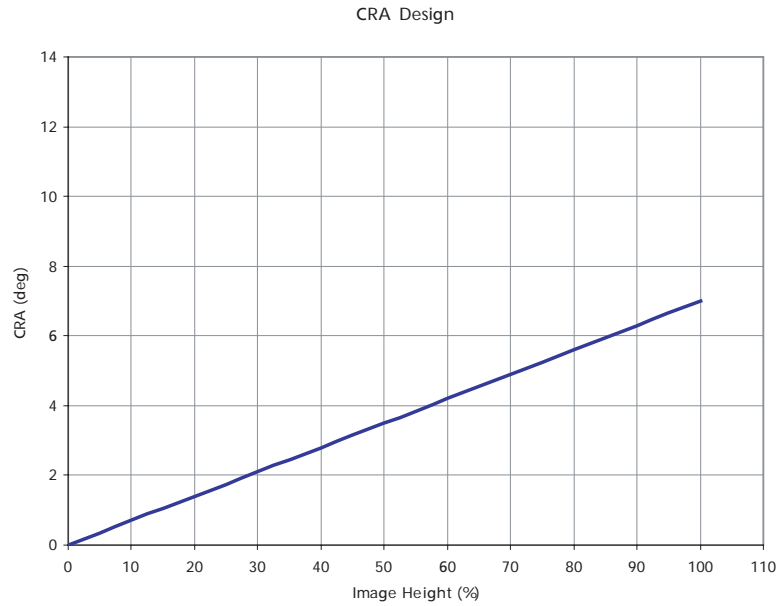
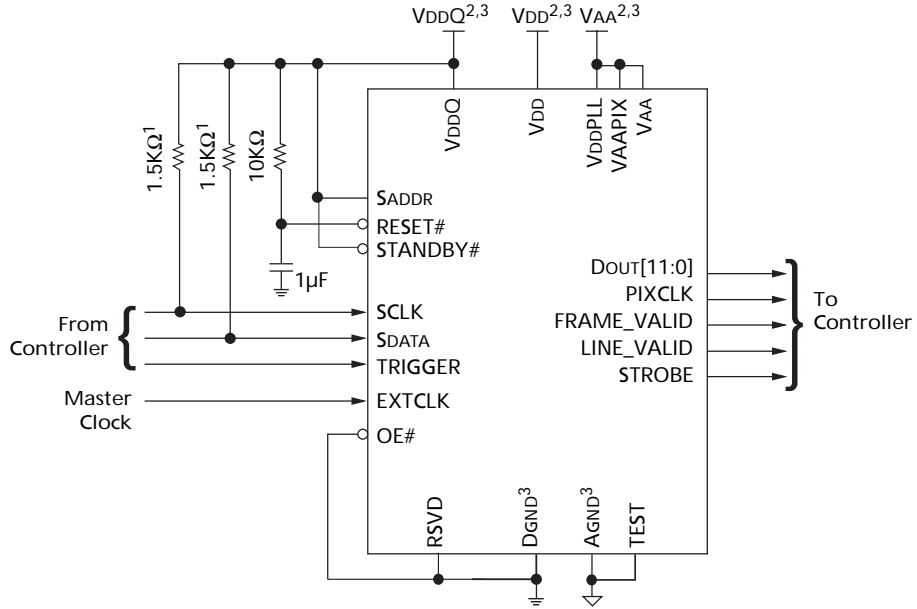


Figure 2: Chief Ray Angle





**Figure 4: Typical Configuration (connection)**



- Notes:
1. Resistor value 1.5KΩ is recommended but may be greater for slower two-wire speed.
  2. All power supplies should be adequately decoupled.
  3. All DGND pins must be tied together, as must all AGND pins, all VDDQ pins, and all VDD pins.

**Figure 5: 48-Pin iLCC 10x10mm Package Pinout Diagram (top view)**

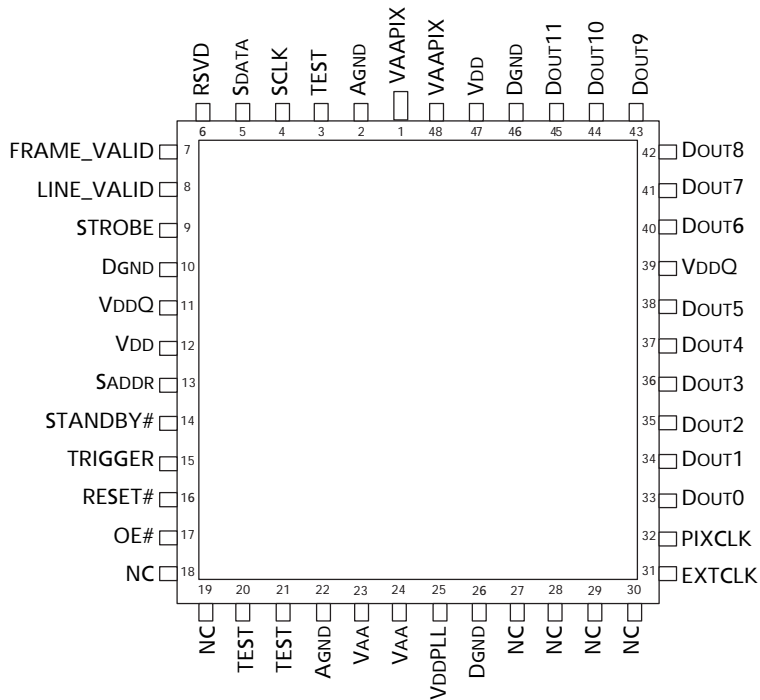




Table 2: Pin Descriptions

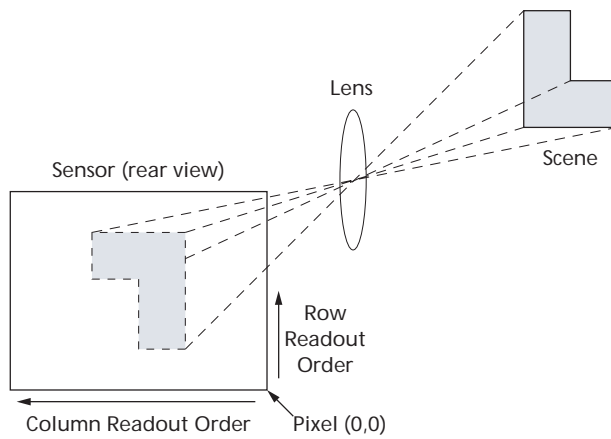
Name	LLCC Pin	Type	Description
RESET#	16	Input	When LOW, the MT9P031 asynchronously resets. When driven HIGH, it resumes normal operation with all configuration registers set to factory defaults.
EXTCLK	31	Input	External input clock.
SCLK	4	Input	<b>Serial clock:</b> Pull to VDDQ with a 1.5K $\Omega$ resistor.
OE#	17	Input	When HIGH, the PIXCLK, DOUT, FRAME_VALID, LINE_VALID, and STROBE outputs enter a High-Z. When driven LOW, normal operation resumes.
STANDBY#	14	Input	<b>Standby:</b> When LOW, the chip enters a low-power standby mode. It resumes normal operation when the pin is driven HIGH.
TRIGGER	15	Input	<b>Snapshot trigger:</b> Used to trigger one frame of output in snapshot modes and to indicate the end of exposure in bulb exposure modes.
SADDR	13	Input	<b>Serial address:</b> When HIGH, the MT9P031 responds to device ID (BA) <sub>H</sub> . When LOW, it responds to serial device ID (90) <sub>H</sub> .
SDATA	5	I/O	<b>Serial data:</b> Pull to VDDQ with a 1.5K $\Omega$ resistor.
PIXCLK	32	Output	<b>Pixel clock:</b> The DOUT, FRAME_VALID, LINE_VALID, and STROBE outputs should be captured on the falling edge of this signal.
DOUT[11:0]	33 to 45	Output	<b>Pixel data:</b> Pixel data is 12-bit. MSB (DOUT11) through LSB (DOUT0) of each pixel, to be captured on the falling edge of PIXCLK.
FRAME_VALID	7	Output	<b>Frame valid:</b> Driven HIGH during active pixels and horizontal blanking of each frame and LOW during vertical blanking.
LINE_VALID	8	Output	<b>Line valid:</b> Driven HIGH with active pixels of each line and LOW during blanking periods.
STROBE	9	Output	<b>Snapshot strobe:</b> Driven HIGH when all pixels are exposing in snapshot modes.
VDD	12, 7	Supply	<b>Digital supply voltage:</b> Nominally 1.8V.
VDDQ	11, 39	Supply	<b>IO supply voltage:</b> Nominally 1.8V or 2.8V.
DGND	10, 26, 46	Supply	Digital ground.
VAA	23, 24	Supply	<b>Analog supply voltage:</b> Nominally 2.8V.
VAAPIX	1, 48	Supply	<b>Pixel supply voltage:</b> Nominally 2.8V, connected externally to VAA.
AGND	2, 22	Supply	Analog ground.
VDDPLL	25	Supply	<b>PLL supply voltage:</b> Nominally 2.8V, connected externally to VAA.
TEST	3, 20, 21	-	Tie to AGND for normal device operation (factory use only).
RSVD	6	-	Tie to DGND for normal device operation (factory use only).
NC	18, 19, 27, 28, 29, 30	-	No connect.

## Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 6). This reflects the actual layout of the array on the die. By default data is first read out of the sensor at pixel (16,54).

When the sensor is imaging, the active surface of the sensor faces the scene, as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced, as shown in Figure 7.

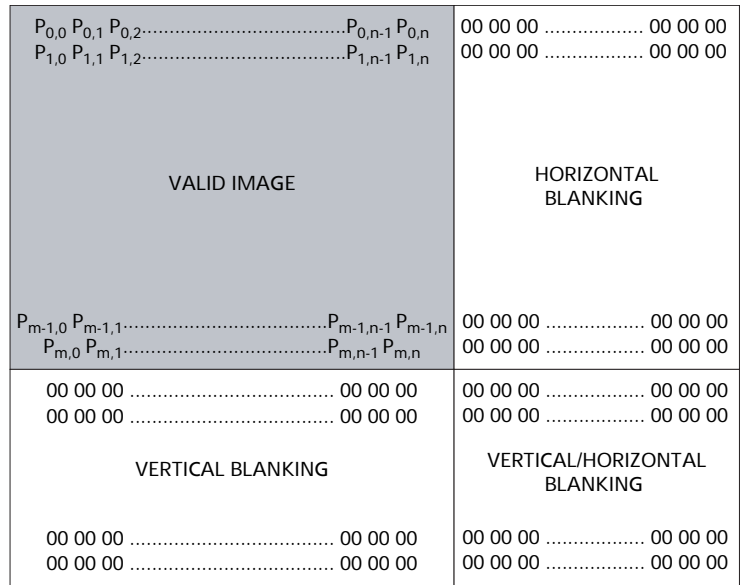
**Figure 6: Imaging a Scene**



**Output Data Format (default mode)**

The MT9P031 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 7. LINE\_VALID is HIGH in the shaded region of the figure.

**Figure 7: Spatial Illustration of Image Readout**



## Readout Modes

### Subsampling

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by two methods: skipping and binning.

Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view. The MT9P031 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of two or three adjacent rows and columns (adjacent same-color pixels). Both 2X and 4X binning modes are supported. Rows and columns can be binned independently.

### Skipping

Skipping reduces resolution by using only selected pixels from the FOV in the output image. In skip mode, entire rows and columns of pixels are not sampled, resulting in a lower-resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skip 3X skips two pairs for each one pair output. Rows and columns are always read out in pairs.

### Binning

Binning reduces resolution by combining adjacent, same-color imager pixels to produce one output pixel. All of the pixels in the FOV contribute to the output image in bin mode. This can result in a more pleasing output image with reduced subsampling artifacts. It also improves low-light performance. For columns, the combination step can be either an averaging or summing operation. Depending on lighting conditions, one or the other may be desirable. In low-light conditions, summing produces a gain roughly equivalent to the column bin factor.

Only certain combinations of binning and skipping are allowed.



## DC Electrical Characteristics

Table 3: DC Electrical Characteristics

Symbol	Definition	Conditions	Min	Typ	Max	Units
V <sub>DD</sub>	Core digital voltage		1.7	1.8	1.9	V
V <sub>DDQ</sub>	I/O digital voltage		1.7	1.8/2.8	3.1	V
V <sub>AA</sub>	Analog voltage		2.6	2.8	3.1	V
V <sub>AAPIX</sub>	Pixel supply voltage		2.6	2.8	3.1	V
V <sub>DDPLL</sub>	PLL supply voltage		2.6	2.8	3.1	V
V <sub>IH</sub>	Input high voltage	V <sub>DDQ</sub> = 2.8V V <sub>DDQ</sub> = 1.8V	2 1.3	-	3.3 2.3	V
V <sub>IL</sub>	Input low voltage	V <sub>DDQ</sub> = 2.8V V <sub>DDQ</sub> = 1.8V	-0.3 -0.3	-	+0.8 +0.5	V
I <sub>IN</sub>	Input leakage current	No pull-up resistor; V <sub>IN</sub> = V <sub>DDQ</sub> or DGND	-	<10	-	μA
V <sub>OH</sub>	Output high voltage	At specified I <sub>OH</sub>	1.3	-	1.82	V
V <sub>OL</sub>	Output low voltage	At specified I <sub>OL</sub>	0.16	-	0.35	V
I <sub>OH</sub>	Output high current	At specified V <sub>OH</sub> = V <sub>DDQ</sub> -400mv at 1.7V V <sub>DDQ</sub>	8.9	-	22.3	mA
I <sub>OL</sub>	Output low current	At specified V <sub>OL</sub> = 400mv at 1.7V V <sub>DDQ</sub>	2.6	-	5.1	mA
I <sub>oz</sub>	Tri-state output leakage current	V <sub>IN</sub> =V <sub>DDQ</sub> or GND	-	-	2	μA
I <sub>DD1</sub>	Digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	-	28	35	mA
I <sub>DDQ1</sub>	I/O digital operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	-	38.6	50	mA
I <sub>AA1</sub>	Analog operating current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	-	72	95	mA
I <sub>AAPIX1</sub>	Pixel supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	-	2.4	6	mA
I <sub>DDPLL1</sub>	PLL supply current	Parallel mode 96 MHz full frame nominal voltage, PLL enabled	-	5	6	mA
I <sub>DD2</sub>	Digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	-	15	35	mA
I <sub>DDQ2</sub>	I/O digital operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	-	6.4	50	mA
I <sub>AA2</sub>	Analog operating current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	-	69	95	mA
I <sub>AAPIX2</sub>	Pixel supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL Enabled	-	3.4	6	mA
I <sub>DDPLL2</sub>	PLL supply current	Parallel mode 96 MHz 4X binning nominal voltage, PLL enabled	-	5	6	mA
I <sub>STBY1</sub>	Hard standby current PLL enabled	EXTCLK enabled	-	<500	-	μA
I <sub>STBY2</sub>	Hard standby current PLL disabled	EXTCLK disabled	-	<50	-	μA
I <sub>STBY3</sub>	Soft standby current PLL enabled	EXTCLK enabled (PLL enabled)	-	<500	-	μA
I <sub>STBY4</sub>	Soft standby current PLL disabled	EXTCLK enabled (PLL disabled)	-	<500	-	μA



Table 4: Power Consumption

Mode	Full Resolution (14 fps)	4X Binning	Units
Streaming	381	262	mW

Table 5: Absolute Maximum Ratings

Symbol	Definition	Min	Max	Units
VDD_MAX	Core digital voltage	-0.3	1.9	V
VDDQ_MAX	I/O digital voltage	-0.3	3.1	V
VAA_MAX	Analog voltage	-0.3	3.1	V
VAAPIX_MAX	Pixel supply voltage	-0.3	3.1	V
VDDPLL_MAX	PLL supply voltage	-0.3	3.1	V
VIN_MAX	Input voltage	-0.3	VDDQ + 0.3	V
IDD_MAX	Digital operating current	-	35	mA
IDDQ_MAX	I/O digital operating current	-	100	mA
IAA_MAX	Analog operating current	-	95	mA
IAAPIX_MAX	Pixel supply current	-	6	mA
IDDPLL_MAX	PLL supply current	-	6	mA
TOP <sup>2, 3</sup>	Operating temperature	-30	70	°C
TST	Storage temperature	-40	125	°C

- Notes:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  2. In order to keep dark current and shot noise artifacts from impacting image quality, care should be taken to keep TOP at a minimum.
  3. Measure at junction.

